



Xinetics / OEM  
Modular Switching Driver Chassis  
Operators Manual

With Revision B backplane, no auxiliary bias

Initial Release 2/23/10

# Table of Contents

Page 3	-	Quick Start Instructions
Page 3	-	Introduction
Page 4	-	System Specifications
Page 5	-	Notable Features
Page 7	-	Front Panel View
Page 8	-	Rear Panel View
Page 9	-	Interface Options
Page 9	-	Control Bus Connector Specification
Page 10	-	SOR-422U Input Bus Connector Specification
Page 12	-	Driving the LVDS Bus
Page 15	-	XiBus Interface
Page 19	-	480 Channel Sub-chassis Architecture
Page 22	-	System Configuration
Page 25	-	LCD Status Displays
Page 27	-	Driver Modes
Page 28	-	Driver Defaults
Page 29	-	Driver Shutdown Mechanisms
Page 31	-	Calibration
Page 32	-	Output Connector Pin Outs
Page 34	-	Driver Limitations
Page 37	-	Command Set
Page 51	-	Manufacturing Mode Commands
Page 54	-	Glossary of Terms

# Modular Switching Driver Operators Manual

This manual applies to the Rev. B Backplane.

## QUICK START INSTRUCTIONS

1. Connect to the RS-232 port on the backplane using a standard RS-232 cable.
2. Connect other end of RS-232 cable to a computer with equipped with Hyperterminal. Use the following settings for Hyperterminal: Baudrate: 115200, databits: 8, parity: none, stopbits: 1, flowcontrol: none.
3. Plug in the Gen III, it will turn on.
4. All LEDs on the front panel should go from red to yellow/orange. If they do not, cycle the power a few times. If all LEDs still do not change to yellow/orange after a few power cycles and remain red, contact Xinetics.
5. At this point, the driver is ready for commands. By issuing an ASCII '1' with Hyperterminal, the bias will go up to -25 V in TEST mode. Attach a DMM to the front panel banana jacks to verify.
6. Issue a '0' command to ramp down the bias and go back into STANDBY mode.
7. Refer to the rest of the manual, and the Command Set section for more information on how to frame data in and utilize additional features of the driver. If any part of this procedure could not be accomplished, call Xinetics.

## Introduction

The Xinetics OEM Modular Switching Driver is a 4U rack based system designed specifically to drive Xinetics deformable mirrors. The chassis consists of a modular power supply, a high speed backplane with integrated controller and up to ten 48 channel driver cards.

The driver amplifier technology incorporated in this system is based on a switching amplifier chipset. This chipset contains an embedded DSP power processor which generates switching drive signals based on 24 bit digital delta sigma conversion. The other chip in the set is an intelligent FET driver which controls the half bridge output stage. Each chipset provides 6 fully digital amplifier channels. The driver card architecture uses 8 chipsets to provide 48 discrete channels per card.

This amplifier system was developed to meet the needs of increased efficiency and packaging density. It operates at a typical efficiency of 93% and dissipates approximately 0.8 watts per channel. The output current capability is approximately 3 amps per channel. With a 1 microfarad load, the slew rate of the amplifier is approximately 6 volts per  $\mu$ sec. System latency is less than 30 microseconds.

# Specifications

Number of channels:	48 – 480 (1 – 10 cards)
Power Dissipation:	1 watt per channel
Input Voltage:	110 Vac / 47-63 Hz
Ambient Temperature:	0 – 30° C
Resolution:	16 Bits
Output Swing:	± 30 volts
Output Current:	± 3 Amps
Slew Rate:	6 volts per microsecond (1 microfarad load)
Frame Rate (Command)	100 Hz (480 Ch)
Frame Rate (Input Bus)	4 KHz (480 Ch), load dependent
Bias Voltage Range	-25 to -70V
Bias Supply Current	limited to 5.5A
Bias Resolution	16 Bits
Bias Read back resolution	10 Bits
Offset Range	±2.5 volts
Offset Resolution	5 mV / LSB
Gain Range	128 dB
Gain Resolution	0.5 dB / LSB

# Notable Features

There are several features incorporated in this latest iteration of the Xinetics digital switching driver system embedded processor code. This code rev. applies to the REV. B backplane hardware only.

The first key change over previous systems (Rev. A Backplane) is that the frame buffer is non-volatile now. The frame buffer is only set to mid scale during the CONFIG cycle. When the user writes a frame to the input buffer, it will remain there until changed.

Another feature incorporated into this latest driver system is voltage table averaging. Every sensor in the system is averaged 32 times before being reported, every voltage read back is averaged 64 times before being reported. This results in very accurate read backs with minimal noise.

Closed loop PID control of the bias voltage has been incorporated. The bias control loop continuously monitors the bias voltage and compares it to a target value. The bias voltage is dynamically controlled based on the load. This loop also provides smooth ramping of the bias voltage for any change required. Regulation loop bandwidth is approximately 80 KHz.

Closed loop PID control of the fan speed has been incorporated.

The back plane can control its own fan tray based on the temperature sensor read backs. Normally the fans run at a fairly slow speed (about 20%) to move enough air through the chassis to allow for closing the temperature loop. The fan control loop continuously monitors the average value of all temperature sensors in the chassis and controls the fan speed to maintain an exhaust temperature of 85° F. The loop will regulate the fan speed to maintain a 10° F rise from inlet to outlet. In the event that the outlet temperature rises above 85° F, the fans will speed up proportionally to move more air and maintain the balance.

There is now an integrated LCD on PSU for at a glance status. The LCD defaults to a context sensitive mode however, commands are provided to allow a rolling display mode for complete status. The contrast and brightness of the display can be controlled via the command bus.

A current limited bias test point has been provided for accurate measurement of the main bias voltage on the mirror using an external DVM.

A blackout mode has been incorporated to allow all light from the driver (LED's and LCD back light) to be turned off to prevent light pollution in light sensitive environments. The operation of the LED's has been changed to show a failure with red, active/no failure with green, and standby with orange/yellow.

An auxiliary high speed input bus (known as the Xibus) has been incorporated which is used for application specific interfaces. In addition to the standard SOR-422U input bus, this Xibus is a SERDES based input designed to accommodate rider board interfaces for FPDP, channel link,

USB 2.0 and other future input mediums. It also allows several daisy-chaining modes for multiple chassis configurations.

Universal Power capability has been incorporated. The PSU is modular and can be designed for virtually any input voltage required. The PSU hardware shipped with this version is set up for 110 Vac.

Automatic system mapping of driver cards is performed during the CONFIG cycle, allowing up to 10 boards to be installed.

## Front Panel:



The modular switching driver is housed in a standard 4U rack chassis. Each card in the chassis has a multicolor LED in the front panel to provide at a glance status. The meanings of the LED's are as follows.

### AC Power ON (Configuration Cycle):

RED	Driver hardware failure.
YELLOW	Driver Card POST Passed, Controller has mapped the driver card.

### Normal Operation:

RED	Driver card hardware failure.
YELLOW	Normal operation, Card activated by command
GREEN	Normal operation, Card idled by command

There is also an optional 1U fan tray available for this system.

**Rear Panel:**





## Interface Options

The Gen III has the following interface options for commanding, data framing, and health/status:

1. Control Bus—A standard RS-232 serial port on the back plane. The Gen III can send and receive commands and health/status.
2. Input Bus—A high speed bus that incorporates the SOR-422U input protocol described later in this manual. This bus can only receive voltage frames, it cannot provide health and status. In order to activate the input bus, the user must turn it on by using the ‘Y3’ command via the Control Bus (RS-232).
3. XiBus Interface—A bus that allows multiple chassis to be daisy chained.

These interfaces are described in greater detail in the following pages. The commands themselves are covered later in the ‘Command Set’ section. This section will cover the physical interface only.

### Control Bus

The control bus is a bidirectional serial RS-232 port through which the driver can be commanded and status returned. All control functions can be executed via ASCII commands with Windows Hyperterminal or a similar terminal emulator program.

There are two ways to determine if the driver is ready for commands after it has been powered on. The first is to visually look at the driver. All the LEDs will turn from red, to orange when the driver is ready. The second way is to poll the driver by using an ‘S’ or ‘send status packet’ command (see Command Set definitions in the back of this manual). After sending the ‘S’ command, the user should wait until a response is received. During the CONFIG cycle, the control bus UART ISR is disabled. The first command sent to the driver will be kept in the UART receiver data holding register and an interrupt request will be issued to service the buffer. Once the CONFIG cycle has completed, the interrupt system will be initialized and the pending interrupt request from the UART receiver will be acknowledged by the embedded control software. A status packet will then be transmitted from the driver to the user. It is important that after the initial ‘S’ command/status request is issued, the user must wait for the driver to respond to the request. If multiple commands are issued, the embedded controller software will see an overrun error from the UART and flush the command request, therefore, no response will be generated.

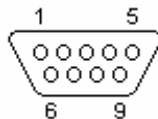
When the driver is ready, then the status request will be answered and the control program can check driver status. Once the driver READY status bit gets set to a 1, the driver has passed all tests and is ready to receive commands. When a command is sent to the driver over the control bus, the user must wait for the appropriate response (ACK, NACK or a frame of data). During the time that the driver system is processing a command, the control bus is ignored. The driver will accept commands only when it is not busy. If a new command is sent before the previous one is ACKed, then a NACK will be generated and the buffers will be flushed.

Each time a command is processed successfully either the requested data or an ‘>’ (ACK) will be sent as an acknowledgement. If a ‘?’ (NACK) is received; the driver did not process the command. When a command is sent to the driver, either the response will be transmitted or the ACK character will be transmitted, the control bus is inactive during command processing so the control software should wait for the ACK, NAK or the correct response before sending another command to the driver, otherwise, the command will be ignored and synchronization may be lost.

Not all commands respond with an ACK, if the command results in a response from the driver (such as asking for a voltage table) then the control program must count bytes to determine when the operation is complete. See the Command Set section in the back of this manual for more specific information about each command and the driver’s response.

DB-9 Pinout on Backplane	RS-232 Signal
2	Transmit Data OUT
3	Receive Data IN
5	Signal Ground

CONTROL BUS CONNECTOR ON BACKPLANE, DB-9 Pin



Use a standard serial cable, not a NULL cable.

### SOR-422U Input Bus

In order to activate the Input Bus, the ‘Y3’ command must be sent over the Command Bus RS-232 interface. More information can be found in the Command Set section.

The receivers used in the driver system are National DS90LV048ATMTC type. The DS90LV048A differential line receiver is capable of detecting signals as low as 100mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered on this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver’s ground reference and the receiver’s ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to 3.3V, but exceeding VCC will turn on the ESD protection circuitry which will clamp the bus voltages.

The table below defines the relation between the IDC pin # and the signal name:

<b>IDC RO W #1</b>	<b>SOR-422U SIGNAL NAME</b>	<b>IDC RO W #2</b>	<b>SOR-422U SIGNAL NAME</b>
1	+DATA0	2	-DATA0
3	+DATA1	4	-DATA1
5	+DATA2	6	-DATA2
7	+DATA3	8	-DATA3
9	+DATA4	10	-DATA4
11	+DATA5	12	-DATA5
13	+DATA6	14	-DATA6
15	+DATA7	16	-DATA7
17	+DATA8	18	-DATA8
19	+DATA9	20	-DATA9
21	+DATA10	22	-DATA10
23	+DATA11	24	-DATA11
25	+DATA12	26	-DATA12
27	+DATA13	28	-DATA13
29	+DATA14	30	-DATA14
31	+DATA15	32	-DATA15
33	N/A	34	N/A
35	N/A	36	N/A
37	DGND	38	DGND
39	N/A	40	N/A
41	N/A	42	N/A
43	+CLOCK	44	-CLOCK
45	+ENABLE\	46	-ENABLE\
47	+FRAME\	48	-FRAME\
49	+READY\	50	-READY\

**INPUT BUS CONNECTOR (50 PIN FLAT RIBBON NUMBERING)**

Other pins are not used in this application. Ground may be needed if the common mode voltage is excessive. The LVDS receivers can tolerate a common mode voltage of up to 5 volts. This ground is provided to allow a digital ground connection to the driver for purposes of ensuring that the common mode voltage is not exceeded which will result in signal integrity issues.

## Driving the LVDS Input Bus

The high speed mirror data is fed to the driver chassis via a variant of the SOR-422U standard (U stands for Unidirectional). This variant differs from the standard in that Xinetics had added digital grounds on pin 37 and 38 to allow the input source to be at the same potential as the driver chassis. This ground may or may not be needed depending on the common mode voltage present on the particular electrical environment that the driver is to be operated in. A determination will have to be made as to the benefit of connecting this ground or not. In some situations, the ground may not be desirable due to the potential of creating ground loops.

The LVDS receiver used in this design is a DS90LV048 from National Semiconductor. In order to obtain maximum signal integrity, it should be driven with a current mode driver such as the DS90LV047 or equivalent. By using a current mode driver instead of a voltage mode driver, the terminator on each LVDS input, will convert the current to a voltage. Because the terminators are in very close proximity to the receiver inputs, the voltage that is generated across the termination by the current flowing through it will act as a voltage source to the LVDS receiver and signal integrity will be optimized.

Another major bandwidth limiting factor is the ability of the LVDS transmitter on the user end to supply enough current to drive the cable capacitance. Xinetics has made the effort to place the LVDS receivers in close proximity to the connectors to minimize stray capacitance. It is recommended that the connection to the driver be made with low capacitance ribbon cables and the cable length be kept to a minimum.

It is practical to assume that a bus speed of about 30 MHz is achievable without extraordinary LVDS bus drive design techniques.

When choosing cables and connectors for LVDS it is important to remember:

1. Use controlled impedance media. The cables and connectors you use should have a differential impedance of about 100 ohms. They should not introduce major impedance discontinuities that cause signal reflections.
2. Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.
3. For cable distances  $< 0.5\text{m}$ , most cables can be made to work effectively. For distances  $0.5\text{m} < d < 10\text{m}$ , CAT3 twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

As described above, try to use balanced cables (twisted pair, twin-ax, or flex circuit with closely coupled differential traces). The creators of LVDS intended it to be used over a wide variety of media. The exact media is not specified in the LVDS Standard. The intention was to leave that

aspect to the referencing standard that specifies the complete interface. This includes the media, data rate, length, connectors, functions and pin assignments. In some applications that are very short (<0.3m), ribbon cable or flex circuit may be acceptable. In box-to-box applications, a twisted pair or twin-ax cable would be a better option due to robustness, shielding and balance. Whatever cable you do choose, following these suggestions will help you achieve optimal results.

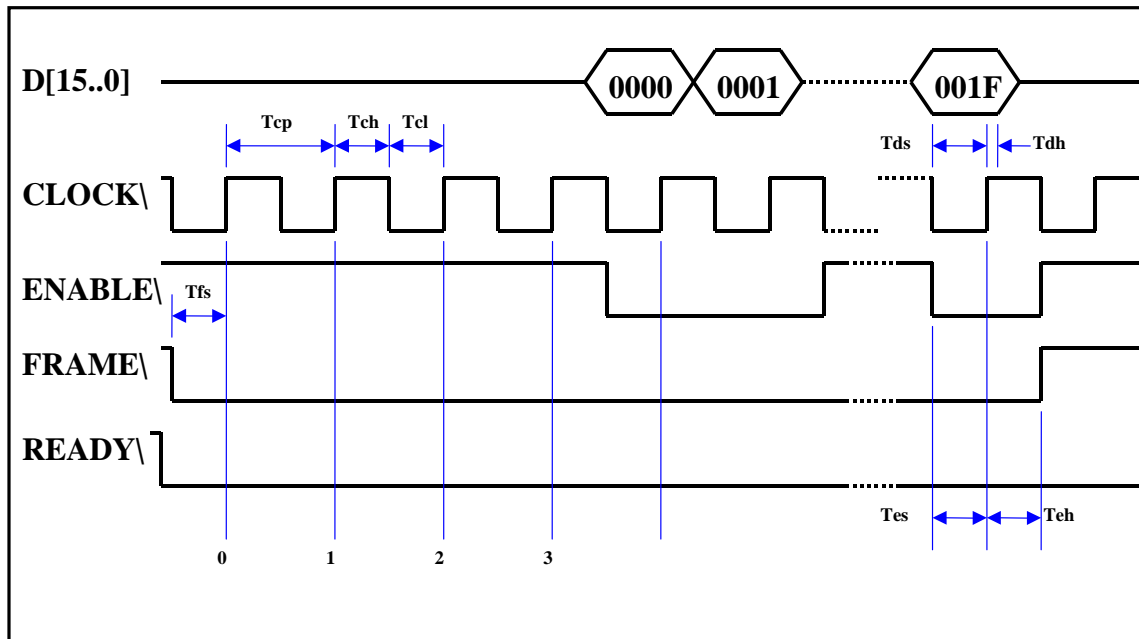
The SOR-422U protocol utilizes the sixteen data lines to transfer the data and four control signals to tell the receiver when there is valid data on the bus for capture. The device sending the data will be referred to as the transmitter (TX) and the receiving device (driver chassis) will be referred to as the receiver (RX).

The signal names and their function are:

- CLOCK** Free running, 50% duty cycle, clock used to synchronize the data.
- ENABLE\** Tells the RX there is valid data during an active frame transfer (Active Low).
- FRAME\** Tells the RX when a block of data is being sent (Active Low).
- READY\** Tells the RX that a valid link to the source device exists (Active Low).
- DATA[15..0]** These signals are used to carry the data word (16-bits) from the TX to the RX.

Below is a timing diagram that illustrates the SOR-422U variant used in this driver system.

## SOR-422U Timing



**TIMING REQUIREMENTS:**

		<b>MIN</b>
Tcp	Clock Period	40ns
Tch/cl	Clock Period High/Low	20ns
Tds	Data Valid before Tclk LH edge	5ns
Tdh	Data Valid after Tclk LH edge	5ns
Tes	Enable Active before Tclk LH edge	5ns
Teh	Enable Active after Tclk LH edge	5ns
Tfs	Frame Active before Tclk LH edge	5ns

## XiBus Interface

The Xibus interface is the system that Xinetics uses to connect multiple chassis together for daisy chain purposes as well as connecting custom interface electronics to the system. Normally the customer only has access to the SOR-422U input bus for high speed mirror data. The Xibus interface is typically for in house use only.

The Xibus interface consists of a SERDES interface as well as several parallel control busses; The SERDES is used to minimize the number of connections on the bus. The connector pinout is described below; it is a 36 pin MDR connector.

PIN NUMBER	PIN NAME	FUNCTION
1	CL_X0-	SERDES DIFFERENTIAL X0-
2	CL_X0+	SERDES DIFFERENTIAL X0+
3	GND	INNER SHIELD
4	GND	INNER SHIELD
5	CL_X1-	SERDES DIFFERENTIAL X1-
6	CL_X1+	SERDES DIFFERENTIAL X1+
7	GND	OUTER SHIELD
8	GND	OUTER SHIELD
9	CL_X2-	SERDES DIFFERENTIAL X2-
10	CL_X2+	SERDES DIFFERENTIAL X2+
11	GND	DIGITAL GROUND
12	GND	DIGITAL GROUND
13	CL_CLK-	SERDES DIFFERENTIAL CLOCK-
14	CL_CLK+	SERDES DIFFERENTIAL CLOCK+
15	GND	DIGITAL GROUND
16	GND	DIGITAL GROUND
17	IB_RX+	INPUT BUS LVDS RCVR +
18	IB_RX-	INPUT BUS LVDS RCVR -
19	GND	DIGITAL GROUND
20	IB_TX+	INPUT BUS LVDS TX +
21	IB_TX-	INPUT BUS LVDS TX -
22	GND	DIGITAL GROUND
23	CID_0	CHASSIS ADDR BUS BIT 0
24	CID_1	CHASSIS ADDR BUS BIT 1
25	CID_2	CHASSIS ADDR BUS BIT 2
26	CID_3	CHASSIS ADDR BUS BIT 3
27	CID_4	CHASSIS ADDR BUS BIT 4
28	CID_5	CHASSIS ADDR BUS BIT 5
29	CID_6	CHASSIS ADDR BUS BIT 6
30	CID_7	CHASSIS ADDR BUS BIT 7
31	GND	DIGITAL GROUND
32	GLOBAL MUTE IN	DAISY CHAIN NORMAL MUTE
33	CHAIN MUTE	DAISY CHAIN FAILURE MUTE

34	SPARE	
35	GND	DIGITAL GROUND
36	CONNECTION DET.	CONNECTION = 0, OPEN = 1

#### SERDES:

Pins 1 – 16 form the SERDES interface, this bus is implemented as a 20 bit bus using a DS90CR216 deserializer chip. The bit definitions are the same as the SOR-422U interface.

A DS90CR215 chip should be used to drive the SERDES section of the XiBus. If this device is used, then input bits will function as shown in the following table:

SERDES INPUT	EQUIVALENT 422U BIT
TX CLOCK	CLOCK
TX IN 1	D0
TX IN 1	D1
TX IN 2	D2
TX IN 3	D3
TX IN 4	D4
TX IN 5	D5
TX IN 6	D6
TX IN 7	D7
TX IN 8	D8
TX IN 9	D9
TX IN 10	D10
TX IN 11	D11
TX IN 12	D12
TX IN 13	D13
TX IN 14	D14
TX IN 15	D15
TX IN 16	FRAME
TX IN 17	READY
TX IN 18	ENABLE

#### Command Bus:

The next section of the XiBus interface is the serial command bus (pins 17-22). This is an LVDS equivalent to the RS-232 command bus. It is enabled through SW4-6 (master / slave). If the chassis is the bus master, then the command bus I/O will be through the RS-232 interface (J41), if the chassis is a slave, the control bus I/O will be through the LVDS portion of the XiBus. The protocol and baud rate are the same regardless of the data path.



PIN 17	IB_RX+	LVDS CONTROL BUS IN +
PIN 18	IB_RX-	LVDS CONTROL BUS IN -
PIN 19	GND	LVDS GROUND
PIN 20	IB_TX+	LVDS CONTROL BUS OUT +
PIN 21	IB_TX-	LVDS CONTROL BUS OUT -

The LVDS command bus is implemented with a DS90LV019 transceiver.

## **Chassis Address Bus**

The next section of the XiBus is the chassis address bus; it is used to address a specific chassis in the daisy chain. When a frame is received by a chassis, it compares the address on the chassis address bus to the chassis address set on SW-5. If the addresses match, the chassis is addressed and will process that frame. If they don't match the frame is ignored. This allows a daisy chain of up to 255 chassis to be discretely addressed. The chassis address bus is single ended 5 volt TTL logic and is terminated with an 8.2K resistor to digital ground.

## **Daisy Chain control**

The final part of the XiBus is for inter-chassis communications. Pin 32 is the normal way that the bus master controls each chassis in the daisy chain. When this line is high, the daisy chain is active, if the bus master pulls pin 32 low, it will cause each chassis in the chain to return to stand by mode. This line is unidirectional and only driven by the bus master.

Pin 33 is the failure mode shutdown pin. It is an open collector line that is passively pulled high by each backplane in the daisy chain. If a failure occurs in any chassis, it will pull pin 33 low. This will cause all of the chassis in the daisy chain to enter stand by mode. This line is only low if a failure is detected in a member of the daisy chain. It can be driven by any chassis to cause a stand by condition for the entire string.

Pin 34 is a spare pin used for chassis status. It should be always left open in the daisy chain.

Pin 36 is the connection detect pin. The device connected to the input should pull this line low. If the line is high and the Xibus is enabled, an input bus configuration error will be issued. It is only used to detect a connection for the XiBus, the SOR-422U bus can be enabled at any time for non daisy chaining modes.

## 480 Channel sub chassis Architecture

The Xinetics modular switching driver chassis contains a backplane and up to ten 48 channel digital amplifier cards. The basic chassis is a 4U height and a 1U fan tray is also required to allow the driver to control its temperature. If a fan tray is not installed, the user is responsible for proper airflow to maintain cooling. Each channel adds about 1 watt of heat load to the total system dissipation.

Several configuration rules should be observed:

1. As a minimum configuration, there must always be a driver card present in slot 1.
2. There can be no gaps in the driver map, in other words, there can be no driver installed to the right of an open slot.
3. If the controller card detects a configuration error, the driver cannot be put into active mode; the card map on the LCD will show the detected configuration.
4. Do not piston all channels in steps larger than what will amount to 3 amps per channel, which depends on the load. There is insufficient power to supply the high slew commands to all channels and a shutdown will occur. TEST mode is used for large piston commands, if large pistons are required in NORMAL mode, then the current limiter must be reduced to slew rate limit the driver amplifier response.
5. If the fan tray is not installed, set SW4-4 to DOWN.

### Backplane / Controller

The backplane consists of an embedded controller, the high speed interfaces and an LVDS system for communication with the driver cards. The backplane interfaces to a modular power supply unit and has the ability to control a fan tray. There is no external bus on the controller processor, all functionality is provided internally by the ST-10. Major functions include:

1. Provide a bidirectional serial interface for the control bus.
2. Initialize the driver cards and map the system.
3. Exchange frames with each driver card via the high speed SSC bus.
4. Monitor voltages and temperatures for proper operation of the system.
5. Control the fan tray.
6. Drive the LCD.
7. Monitor differences between the input data and the output voltages for tracking.
8. Control the functions of the high speed bus.
9. Control the main and bias generator.

## **Driver Card**

The driver card contains the embedded processor which runs the control program out of flash memory. The functions of the embedded processor are listed below:

1. Digitize all power supply rails and temperature sensors.
2. Digitize all output voltages.
3. Provide bidirectional high speed communications with the controller.
4. Monitor temperatures and amplifier performance, protect for overloads.
5. Control all operations of the bit stream generator (BSG) FPGA.
6. Receive high speed LVDS mirror data from the LVDS backplane.
7. Control the amplifier parameters and autozero functions.

The embedded processor is configured to drive an external 16 bit multiplexed bus that is used to control the external peripherals not resident on the ST-10 chip. These are the BSG FPGA and the AD7661 read back ADC, I2C bus masters and the MUX system. There are also a large number of port pins used to drive functions in the system like register selects and control signals. Please refer to the block diagram elsewhere in this manual for more information.

## **Bias Generator**

The bias generator is located in the power supply module. It receives PWM signals from the backplane controller and generates a negative bias voltage for the mirror. It also provides feedback to the controller in order to close the bias regulation loop. The bias voltage is continuously monitored by the controller card and the PWM is varied to maintain the desired bias level regardless of current demands of the mirror. If the bias loop ever goes out of regulation or fails, a bit will be set in the status read back reflecting the problem. The bias voltage is also reported in the status table and on the LCD.

## **Bias Voltage Control**

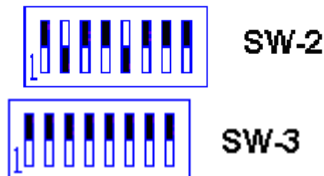
Normally the bias voltage applied to the mirror is set up at Xinetics according to the mirror type. Some customers prefer to change the bias level on the mirror to suit their specific application. The modular driver system provides the ability to set the mirror bias to any level between -25 and -70 volts. Caution should be exercised when modifying the bias voltage because if the bias voltage is set less than the negative amplifier swing, the actuator can be reverse biased and suffer stroke degradation.

The normal bias level for a modular mirror is approximately -50 volts. The driver will default to a bias voltage of -25 volts in TEST mode and -50 volts in NORMAL mode. In TEST mode, the output amplifier can swing  $\pm 15$  volts resulting in a maximum drive voltage of 10 to 40 volts, in NORMAL mode, the output amplifier can swing  $\pm 30$  volts which results in an actuator operating range of 20 to 80 volts.

The bias voltages must be ramped up and down smoothly when applied to the mirror. The embedded controller has been programmed to apply the bias by ramping the voltage. This is done when the START command (0x31) is sent to the control bus.

## System Configuration and the Chassis Address Switch

There are several configuration switches on the backplane of the driver chassis. Two of these switches (SW2 and SW3) are used for microprocessor operating modes and should never be changed. The default configuration is given below in the event of inadvertent changes. They both must be set up as shown for proper operation.



SW3-5 is the bootstrap loader switch; it is used when an upgrade to the FLASH memory is required. Normally this switch will be set to DOWN but new firmware can be loaded through the command bus if this switch is UP.

Switch-4 is the configuration switch:



Factory Default Configuration

- SW4-1 = BAUD RATE SEL - 0
- SW4-2 = BAUD RATE SEL - 1
- SW4-3 = PROTECTION ENABLE
- SW4-4 = FAN CONTROL ENABLE
- SW4-5 = ENABLE AUX BIAS GEN
- SW4-6 = MASTER / SLAVE
- SW4-7 = STREAM STATUS TABLES
- SW4-8 = STREAM VOLTAGE TABLES

Baud rate select		
SW4-1	SW4-2	Control Bus Baud Rate
U	U	19,200
D	U	38,400
U	D	57,600
D	D	115,200

### Protection Enable

If SW4-3 is set to UP, the driver will monitor temperatures and voltages and shut down if a problem is detected. If SW4-3 is set to DOWN, the driver will only shutdown if a catastrophic failure is detected, such as a power supply rail failure.

#### Fan Control Enable

If SW4-4 is set to UP, the driver will control its own fans to maintain proper cooling and monitor fan status. If SW4-4 is set to DOWN, the driver will not expect to see a fan tray installed. This is used when the customer is providing their own rack cooling solution or for multi chassis installations (discussed later in this manual).

#### Auxiliary bias generator (not installed)

SW4-5 is set to UP.

#### Master / slave

If SW4-6 is set to DOWN, the driver chassis is considered to be the daisy chain bus master. Control bus I/O is via the RS-232 connector on the backplane. If SW4-6 is set to UP, the chassis is in slave mode, the control bus I/O is via the LVDS portion of the XiBus and the chassis address bus must match the chassis address set into SW% for the chassis to be considered “addressed”.

#### Streaming modes

If SW4-7 is set to DOWN, then the driver will stream status tables out of the control bus port. If SW4-8 is set to DOWN, then the driver will stream voltage tables out of the control bus port. If both switches are set to DOWN, then the driver will alternately stream status and voltage tables. In order to enable this mode, the switches must be set up before power is applied. The driver will wait for a byte on the control bus before streaming begins. While data is streaming, the control bus will still accept all commands except for an S or a V.

#### Note:

SW4 is only sampled during the configuration cycle. If it is changed, the driver must execute another configuration cycle for the new settings to take affect. A configuration cycle can be initiated by either cycling the driver power or depressing the manual reset button (SW1). The driver should be in STANDBY mode before initiating a reset. However, the real time switch setting will be returned any time a status request is initiated.

SW-5 is the chassis address switch; it is set to all ON for a chassis address of 0. This is the normal stand alone mode. If the chassis address is zero, then the chassis is programmed to be the daisy chain bus master. The binary value of this switch is added to the card slot address at CONFIG time.

If SW5 is set to 11111111B (all UP) then the first channel in the card map is channel 0, if SW5 is set to 11111110B then the first channel in the chassis is mapped to channel 480. For non daisy chained mode, SW5 should always be set to 11111111B. The value of SW5 is displayed on the LCD as the CHASSIS ADDRESS.



SW-5

Default Setting—  
Set to an address of 0 (master)  
Card map runs from 0 to 479



SW-5

Set to an address of 1  
Card map runs from 480 to 959

SW5 is shown to make the chassis the bus master and is also set to 11111111B for non daisy chained mode.

At power up time, the switch value is added to the driver board slot ID to determine the channel address of the chassis. For example, if the chassis address is set to 0, then the input frame will begin at channel 0 and continue up to channel 480 (if all 10 boards are installed). If the chassis address is set to 1, then the channel map will begin at channel 481. This switch is used for configuring a multi chassis system using daisy chain mode with the XIBUS. Up To 255 chassis may be daisy chained using this addressing scheme.



## Status Display

The LCD on the front of the PSU is used for at a glance status as well as manufacturing setup. The accuracy of the voltmeter and temperature displays is typically  $\pm 5\%$ . They are intended to provide a rough idea of system performance. There are high accuracy test points provided if a particular parameter must be measured to high precision. The bias test point on the front of the PSU is provided to allow very accurate setting of the mirror bias voltage with an external DVM.

### (0) Chassis Status Display

Line 1 CARD MAP xxxxxxxxxx  
Line 2 CHASSIS ID = nnn  
Line 3 BIAS VOLTAGE = nnnV  
Line 4 STATUS LINE



```
CARD MAP 1111111111
CHASSIS ID = 0
CHANNELS MAPPED 480
DRIVER ACTIVE
```

### (1) Card Map Display

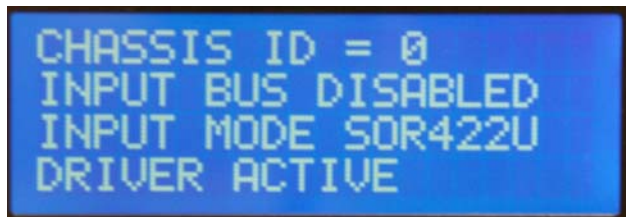
Line 1 SLEW MONITOR XXX  
Line 2 BIAS VOLTAGE = nnnV  
Line 3 CURRENT LIMIT = 50%  
Line 4 STATUS LINE



```
SLEW MONITOR OFF
BIAS VOLTAGE = 47V
CURRENT LIMIT = 50%
DRIVER ACTIVE
```

### (2) Bus Mode Display

Line 1 CHASSIS ID = nnn  
Line 2 INPUT BUS ENABLED  
Line 3 INPUT MODE SOR-422  
Line 4 STATUS LINE



```
CHASSIS ID = 0
INPUT BUS DISABLED
INPUT MODE SOR422U
DRIVER ACTIVE
```

### (3) General Info Display


Line 1 BAUD RATE = 115,200  
Line 2 FAN CONTROL ON  
Line 3 PROTECTION ENABLED  
Line 4 STATUS LINE



```
BAUD RATE = 115,200
FAN CONTROL ENABLED
PROTECTION ENABLED
DRIVER ACTIVE
```

### (4) Cooling Status Display \*

Line 1 P. S. TEMP = nnnC  
Line 2 FAN SPEED = nnn%  
Line 3 CHANNELS MAPPED nnn



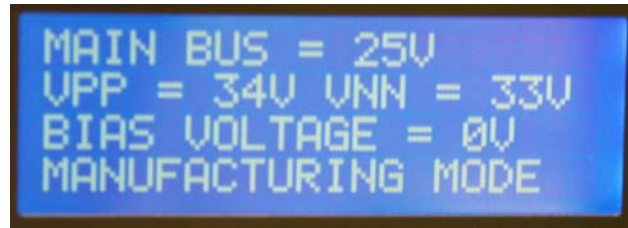
```
P. S. TEMP = 22C
FAN SPEED = 22%
BIAS VOLTAGE = 0V
MANUFACTURING MODE
```

(5) Bias Status Display \*

Line 1 I LIMIT = nn Ma  
Line 2 BIAS VOLTAGE = nnnV  
Line 3 +24 VOLT RAIL = nnnV  
Line 4 STATUS LINE

(6) Supply Status Display \*

Line 1 +24 VOLT RAIL = nnnV  
Line 2 VPP = 34V, VNN = 34V  
Line 3 BIAS VOLTAGE = nnnV  
Line 4 STATUS LINE



(7) Software Status Display\*

Line 1 B. P. CODE REV. 1.4  
Line 2 DRIVER CODE REV. 1.0  
Line 3 DRIVER FPGA REV. 1.3  
Line 4 STATUS LINE



When power is applied to the driver system, each driver card will perform a power on self test. During this time, the front panel LED is RED. If the test fails, the led stays RED. At this point, all the driver cards signal the controller that they are ready and wait for the controller to send each board a slot ID. When the driver card is mapped and a slot ID is received, the driver card LED will turn YELLOW, the driver system will exit CONFIG mode and enter STANDBY mode. Default calibration coefficients will be loaded into the gain tables and the power amplifiers will be enabled, also the bias voltage will be set to 0 volts resulting in zero voltage actively driven on each actuator.

## Driver Modes

There are five modes the system can operate in. These modes are CONFIG, STANDBY, TEST, MANUFACTURING, and NORMAL mode. Normally the driver will automatically exit the CONFIG mode and enter STANDBY mode on start up unless there is a hardware problem. When the driver is in CONFIG mode, the control bus is disabled. After configuration, the driver is put into standby mode. When an ASCII '1' (0x31) is sent to the command bus, the driver will enter TEST mode. The amplifiers will be enabled and drive the outputs to mid scale (0 volts) and the bias will be set to approximately -25 volts. Frames can be sent to the driver via the control bus at this point. See the appendix in this manual for the command protocol. MANUFACTURING mode should be used with caution, a more in depth explanation is provided at the end of the manual.

The default power on mode is TEST mode which loads half scale gains and a low bias voltage. To switch to NORMAL mode, the driver must be in STANDBY mode (LEDs orange/yellow) and then the 'MN' command must be issued. Modes can only be changed while the driver is in STANDBY mode. In NORMAL mode, care should be exercised. Depending on the mirror, certain limitations may exist regarding stress on the mirror.

When the driver is running, the embedded processor will check the temperature sensors, power supply rails, and bias for correct values and shutdown the chassis if a problem is detected. There are several levels of protection incorporated in the driver. SW4-3 is the protection enable switch. This switch is used to totally disable the protection systems in situations where the driver can not go down. If SW4-3 is UP, then the system will check temperatures and supply rails and mute the chassis if a problem is detected. If SW4-3 is DOWN, failures will be reported on the LCD and in the status words but the driver will not shut down.

## Driver Defaults

There are several parameters that get set to defaults during a mode change; the table below describes these parameters and their defaults:

PARAMETER	TEST MODE	NORMAL MODE	MFG. MODE
Current Limit	20%	100% (100%)	OFF (100%)
Gains	½ scale	Full Scale	*
Offsets	0	0	*
Frame Ramping	ON	ON	OFF
Main BIAS	25v	70v	*
Aux BIAS	25v	50v	*
LCD	Event Driven	Event Driven	Rolling
LED's	ON	ON	ON
Frame Size	480	480	*

\* The parameter depends on how MANUFACTURING mode was entered.

On power up, the driver will enter TEST mode and the default parameters above will be set up. Most default values can be modified via the control bus.

### Current Limiter

The current limiter is a hardware mechanism (similar to an automatic fuse) that will protect the amplifier in the event of an over current condition. If a situation results in current limiter activation (output short or excessive slew rate), then the system will shutdown and require the entire chassis to be idled and then reactivated (0x30, 0x31). The factory setting for the current limiter is 3 amps for an individual channel. If a different value is desired, please contact Xinetics.

### Latency

It is recommended that if high bandwidth and low settling time are desired, the mirror cables be kept as short as possible.

## Driver Shutdown Mechanisms

The system has two main protection modes determined by SW4-3. When SW4-3 is UP, then protection is enabled, the system will check temperatures and power rails for nominal values, it will also check amplifier status for proper operation. In the event that any of the above checks fails, the system will safe the mirror and then enter STANDBY mode.

If SW4-3 is DOWN, most of the protection systems are disabled. All above checks are still performed and data is reported through the status packet however, the system will not enter STANDBY mode if a parameter goes out of tolerance. If an amplifier fails, then only the five other channels associated with the bad one will be idled. If an over temperature situation occurs, the fans will still be controlled and will ramp to the maximum CFM however, the over temperature condition will not cause a system shutdown.

The table below indicates the various system responses for each condition:

<b>Condition</b>	<b>Protection Enabled</b>	<b>Protection Disabled</b>
<b>Rail out of Tolerance</b>	Chassis Mute	No Action
<b>Communication Failure</b>	Chassis Mute	Board Mute
<b>Amplifier Failure</b>	Chassis Mute	Amplifier Mute (6 channels)
<b>Over Temperature*</b>	Chassis Mute / Fans to MAX	Fans set to MAX
<b>Bias Failure</b>	Chassis Mute	No Action

\* The following temperature thresholds are present in the system:

Fan Temp Monitor:

0-25C – Fans Idle (10%)

25C – 50C Fans Proportionally Controlled up to 100%

50C – over temp alarm issued

60C – System shutdown if protection enabled (fans to 100%) MAX

Notes:

1. The fan speed is controlled by the average of all the temperature sensors in the system. Depending on the configuration, either the average of the board sensors or the temperature of the power supply sensor will determine the fan speed, which ever is greater.
2. Each driver card contains 8 temperature sensors.
3. Each driver card temperature sensor is checked for limits if protection is enabled.
4. All temperature sensors are reported in the status packet

## Multi-Chassis Cooling

A multi-chassis setup is typically housed in a vertical rack cabinet. Special considerations must be given to the “chimney effect”. If each chassis and its respective fan tray are simply stacked one on top of the other, then the heat from the lower chassis will fire into the bottom of the next higher chassis. Xinetics has coped with this issue in a number of ways. The best mechanism is to use a plenum between each chassis assembly to direct the air in such a way as to draw cool air in from the front and discharge the heated air to the rear of the cabinet where it can be exhausted by fans. If this method is used, then each chassis should be configured to control its own fan tray.

If the chimney effect cannot be avoided due to space limitations, then the master / slave mode should be used to control the fans. Assuming that the Xinetics 1U fan tray is used, then each fully populated chassis will produce approximately 10° C rise in exhaust temperature at 1000 CFM. Also note that the inlet temperature should be kept below 55° C to avoid thermal shutdowns. This implies that if ambient temperature is 25°C, a maximum of three chassis can be stacked without regard to the chimney. In this mode, the top chassis should become the fan master and the lower chassis should be configured as slave chassis. To do this, the top chassis (the hottest) should have SW4-4 should be set to UP (enable fan control). On each chassis below the master, SW4-4 should be set to DOWN thus disabling fan control for that chassis. Xinetics can supply a cable to allow the PWM fan control from the master to be distributed to all of the slave fan trays in the system.

**If more than 3 chassis are to be stacked, a plenum must be incorporated to prevent excessive inlet temperatures from being applied to the upper most chassis in the system.**

## Calibration

Driver calibration can be performed by use of the ID, IG and IO commands. The driver system must be in NORMAL mode to be calibrated. When the driver is in TEST mode, only default calibration values are used. The calibration should be performed as follows:

1. Place the driver system in NORMAL mode.
2. Activate the driver and piston all channels to +15 volts (+half scale).
3. Record all voltage table read backs.
4. Piston all channels to -15 volts (- half scale).
5. Subtract these voltage table read backs from the first set, the result is the gain span.
6. Calculate the gain factor for each channel to set the span to 30 volts.
7. Write the new gains using the IG command.
8. Set all channels to mid-scale.
9. Record all voltage table read backs.
10. Calculate the offset frame to bring all channels to mid-scale.
11. Write in the offset frame using the IO command.

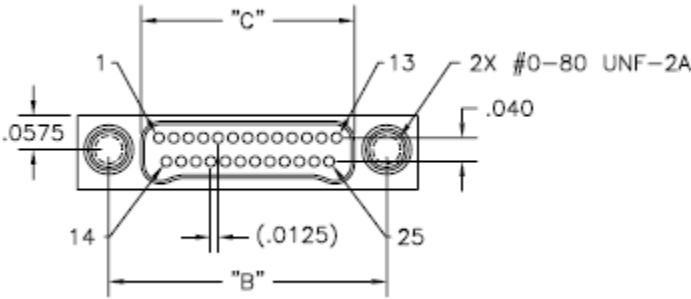
The above procedure will calibrate the driver for a full scale span of  $\pm 30$  volts and reduce the offsets to match the channels. Typical values for gain range from 0xE0 to 0xE5 depending on component tolerances. Typical offset values should be within 20-30 counts of zero. There are finite limits to the level of calibration that can be achieved using the internal voltage read back system. As stated previously, each voltage read back value is averaged 64 times on the driver card before being supplied to the controller as a valid voltage value. Depending on the required precision, more averages may be performed by the user over multiple voltage read back frames to lower the apparent noise in the system. The rule of thumb is as the number of frame averages increases, the noise drops by the square root of the number of samples. So if extremely accurate calibration is to be performed, the user can average say 100 frames for each measurement to generate more accurate calibration coefficients. The point of diminishing returns will be reached when the values of calculated gain coefficients are less than 0.5 dB because that is the resolution of the gain factor.

When a calibration is executed, the user should verify that there is sufficient overhead to prevent riling the amplifiers. VPP and VNN are reported in the controller status packet. The amplifiers will operate reliably within 3 volts of the rail. Xinetics ships this system with the rails set to  $\pm 34$  volts which will prevent riling the amplifiers if programmed for a maximum output voltage of  $\pm 30$  volts. If larger spans are required, then Xinetics can set the power supply rails at anything up to  $\pm 40$  volts which would allow a properly calibrated system to swing up to  $\pm 35$  volts at the expense of a slightly increased noise floor and slightly higher power dissipation. It is always preferable to keep the power supply rails as low as possible to increase the MTBF of the system.

# Output Connector Pin Outs

For most Gen III drivers, unless there is a specific customer request for a different configuration, the face sheet connectors are contained on the DMI connected to the backplane. The face sheet requires 177 channels as well as bias therefore; three 48 channel driver cards are dedicated to face sheet drive. The first three boards in the chassis are assigned to the face sheet. The fourth board in the chassis is for the tip tilt stage; this board is different from the face sheet driver cards and should never be interchanged with one. The tip tilt board has increased current capability. The first three DMI cards contain an Omnetics micro D connector for connection to the standard mirror cable. The fourth DMI contains a 37 pin D-sub connector for connection to the tip tilt stage on the mirror. The pin outs for these connectors is shown below.

## Omnetics 51 pin Micro-D Bilobe Connector:



PART NO.	CONTACTS	"A"	"B"	"C"	"D"	"E"
A28300-051	51	.900	.795	.685	.625	.600



PIN	FUNCTION	PIN	FUNCTION
1	CH-1	27	CH-26
2	CH-2	28	CH-27
3	CH-3	29	CH-28
4	CH-4	30	CH-29
5	CH-5	31	CH-30
6	CH-6	32	CH-31
7	CH-7	33	CH-32
8	CH-8	34	CH-33
9	CH-9	35	CH-34
10	CH-10	36	CH-35
11	CH-11	37	CH-36
12	CH-12	38	CH-37
13	CH-13	39	CH-38
14	CH-14	40	CH-39
15	CH-15	41	CH-40
16	CH-16	42	CH-41
17	CH-17	43	CH-42
18	CH-18	44	CH-43
19	CH-19	45	CH-44
20	CH-20	46	CH-45
21	CH-21	47	CH-46
22	CH-22	48	CH-47
23	CH-23	49	CH-48
24	CH-24	50	BIAS
25	CH-25	51	GROUND
26	BIAS	--	NO PIN

## Driver Limitations

The overall system performance depends on several variables including, the PSD of the aberrations that are being corrected, minimum/maximum step sizes, frame rate, actuator type, etc. It is also desirable to minimize the offsets by centering the commands around mid scale since the amplifiers supply less current as their output approaches the rails.

Piston commands place a very large current demand on the bias supply and may cause it to droop. The MCU is programmed to allow a certain amount of sag in the bias supply due to current limitations but will safe the driver if the droop is too large or for too long.

Please note that commands can be sent to the driver that are impossible to perform, for example in a 177 channel system with a 2 microfarad actuator capacitance, a piston command can be issued that will result in 2 amps per channel being delivered to the mirror, most of this current will be delivered by the bulk filter capacitors distributed throughout the system and will result in over 300 amps of pulse current being delivered to the mirror.

The driver has enough reserve energy storage to source or sink a peak of 3 amps of current from each channel for 10 microseconds. If commands require more current, the driver rails will begin to collapse. This will not result in a catastrophic failure but the internal MCU is programmed to disable the driver system in the event of this occurrence.

It is recommended that the protection switch be enabled during the system integration phase in order to prevent hardware failures until the operation of the system has been fully characterized.

The best way to determine the system performance limitations is to start out at small step sizes and slowly increase to the maximum step size needed.

### Precautions

When the mirror is on bias and a shutdown is requested (0x30), the following operations are performed by the embedded processor; the frame buffer is frozen, the frame buffer is ramped down to zero volts. Once the frame buffer is at mid-scale, the bias is ramped to zero. An ACK is transmitted from the control bus, once the ACK is received, the user can then power down the driver system and disconnect the mirror if required. As long as the shutdown sequence is completed, it is safe to remove or install a discharged mirror to the driver system.

It is essential that the mirror be powered up and down correctly to prevent damage to either the driver or the mirror. The driver contains software to ensure smooth ramping of all drive signals to the mirror. Please ensure that the driver system is in standby mode before powering down and connecting or disconnecting any mirror to the unit. When the unit is in standby, it will be driving midscale (0 volts) with a zero reference voltage. This configuration will actively sink any residual charge on the mirror safely and prevent damage to the driver the next time it is powered up.

## **Connecting a mirror to the driver**

Care must be exercised when a mirror is connected to the driver. If the mirror has any residual charge on it, it will discharge into the output amplifiers and possibly damage one or more of them. To connect a mirror to the driver, first ensure that the mirror is discharged by using the shorting connector supplied with the unit. Power on the driver system and verify that it is in standby mode. The discharged mirror can now be safely connected to the driver. As long as the mirror is connected to the driver, the software will ensure proper management of the mirror through power up and down cycles.

## **Removing a mirror from the driver**

To disconnect the mirror from the driver, place the driver system in standby. The software will smoothly ramp down the output channels to mid-scale and then ramp the reference voltage to zero volts. At this time, the mirror can be disconnected and then the shorting plug can be attached to the mirror. The power switch to the driver can be switched off at this point if desired.

## **In case of a power interruption**

In the event that the driver is in active mode and a power interruption occurs, it is essential that the driver system not be re-powered immediately or an SCR latchup might occur on an amplifier. If this occurs, the embedded controller will sense the fault condition and shut down to prevent internal damage. The driver system contains built in bleed resistors on all channels to bleed the charge off the mirror. When the driver is powered on, the outputs of the amplifiers look like a 500 ohm resistor connected to ground. The mirror will be discharged automatically within a few seconds of the driver shutting down. The problem will occur if the power is lost and restored within 1 second. This is longer than the power supply hold up time and shorter than the bleed down time. This window of uncertainty should be avoided.



voltage will give you the total voltage on the output. The following table shows some read backs from the NORMAL mode.

<b>Reported from the Driver, counts, hexadecimal</b>	<b>Reported from the Driver, counts, base 10</b>	<b>Corresponding voltage, not including bias</b>
0xF0F2	61682	30 V
0xB879	47225	15 V
0x8000	32768	0 V
0x4788	18312	-15 V
0x0F10	3856	-30 V

Note these numbers will not be exact, due to analog tolerances for components, and measurements.

**‘S’, 0x53, 01010011B            SEND STATUS TABLE**

RETURNS: 297 bytes total (maximum configuration 10 boards)

Packet length = 297 bytes

‘S’, 0x53, 01010011B	1 BYTE
CONTROLLER STATUS WORD	2 BYTES
CHASSIS STATUS WORD	2 BYTES
MAIN BIAS VALUE	2 BYTES
AUX BIAS VALUE	2 BYTES
24 VOLT RAIL MONITOR	2 BYTES
BACK PLANE TEMP SENSOR	2 BYTES
FAN SPEED	2 BYTES
DIP SWITCHES	2 BYTES
DRIVER1 STATUS TABLE	28 BYTES
DRIVER2 STATUS TABLE	28 BYTES
.	
.	
.	
DRIVER 10 STATUS TABLE	28 BYTES

Byte 0 (‘S’) is the packet identifier followed by the values low byte, high byte.

CONTROLLER STATUS WORD - The bits are defined as follows;

READY	BIT 0	1 WHEN DRIVER READY FOR COMMANDS
ACTIVE	BIT 1	1 WHEN IN ACTIVE MODE (MIRROR ON BIAS)
IBACTIVE	BIT 2	1 IF INPUT BUS ACTIVE
TESTMODE	BIT 3	1 IF TEST MODE
MFGMODE	BIT 4	1 IF SYSTEM IS IN MANUFACTURING MODE
HARDMUTED	BIT 5	1 WHEN DRIVER AMPS ARE SHUTDOWN
BIASVALID	BIT 6	1 WHEN BIAS REGULATION LOOP HAS STABILIZED
ERROR	BIT 7	1 IF AN INVALID COMMAND WAS ISSUED
CONFIGERROR	BIT 8	1 IF THE BOARD CONFIGURATION IS BAD
POWERFAIL	BIT 9	1 IF A RAIL IS OUT OF TOLERANCE
BIASFAIL	BIT 10	1 IF THE BIAS CANNOT BE CONTROLLED
OVERTEMP	BIT 11	1 IF THE SYSTEM IS GETTING TOO HOT
DRIVERFAIL	BIT 12	1 IF THERE IS A HARDWARE FAILURE
FANFAIL	BIT 13	1 IF THE FAN CANNOT BE CONTROLLED
NEARRAIL	BIT 14	1 IF ANY CHANNELS ARE WITHIN 20% OF MAX
SLEWRATEFAIL	BIT 15	1 IF THE CHASSIS IDLED DUE TO SLEW RATES

CHASSIS STATUS WORD - The bits are defined as follows;

BIT 0 ALWAYS = 0  
BIT 1 ALWAYS = 0  
BIT 2 ALWAYS = 0  
BIT 3 ALWAYS = 0  
BIT 4 ALWAYS = 0  
BIT 5 ALWAYS = 0  
BIT 6 1 IF BOARD 1 IS RESPONDING TO CONTROLLER  
BIT 7 1 IF BOARD 2 IS RESPONDING TO CONTROLLER  
  
BIT 8 1 IF BOARD 3 IS RESPONDING TO CONTROLLER  
BIT 9 1 IF BOARD 4 IS RESPONDING TO CONTROLLER  
BIT 10 1 IF BOARD 5 IS RESPONDING TO CONTROLLER  
BIT 11 1 IF BOARD 6 IS RESPONDING TO CONTROLLER  
BIT 12 1 IF BOARD 7 IS RESPONDING TO CONTROLLER  
BIT 13 1 IF BOARD 8 IS RESPONDING TO CONTROLLER  
BIT 14 1 IF BOARD 9 IS RESPONDING TO CONTROLLER  
BIT 15 1 IF BOARD 10 IS RESPONDING TO CONTROLLER

Chassis status always reads 0xFFC0 (bits left justified) for a fully populated chassis:

1111 1111 1100 0000 B  
F F C 0 (HEX)

For a 5 board system, the chassis status word will read 0x07C0:

0000 0111 1100 0000 B  
0 7 C 0 (HEX)

MAIN BIAS VALUE: Must convert to base 10, and subtract from 1023. Then divide by 12.3. This will only report accurately while the bias is up, it will not work in STANDBY mode. It may be off by 4-5% due to rounding errors.

AUX BIAS VALUE: Unused, auxiliary bias not installed. Two bytes will be present in the data stream from the driver, but they can be ignored. Keep this in mind when indexing the commands that follow.

24 VOLT RAIL MONITOR: Must convert to base 10, and divide it by 23.2.

BACK PLANE TEMP SENSOR: Must convert to base 10, and divide by 14.

FAN SPEED: Fan speed is reported in counts. To convert the reported number to a percentage of full strength, use the equation:  $y = -.0058x + 100$ , where  $x$  is the number reported from the driver, and  $y$  is the percentage of fan speed. Fan on full will be 100%. Due to rounding errors, this read back may be off by about 5%.

## DIP SWITCHES

For all dip switches, a return of '0' from the Gen III is 'up', and a return of '1' is 'down.'

Bits 0-7 give the values of Switch 4 (1-8) on the Backplane as follows:

BIT0 = BAUD RATE SEL – 0—Factory default is down/115200 baud

BIT1 = BAUD RATE SEL – 1—Factory default is down/115200 baud

BIT2 = PROTECTION ENABLE—Factory default is up/on

BIT3 = FAN CONTROL ENABLE—Factory default is up/on

BIT4 = ENABLE AUX BIAS GEN—Factory default is up/off

BIT5 = MASTER/SLAVE MODE—Factory default is down/master

BIT6 = STREAM STATUS TABLES—Factory default is up/off

BIT7 = STREAM VOLTAGE TABLES—Factory default is up/off

Bits 8-15 give the chassis address, or Switch 5 (1-8) on Backplane. Factory default is all up:

BIT8 = Switch 5-1

BIT9 = Switch 5-2

BIT10 = Switch 5-3

BIT11 = Switch 5-4

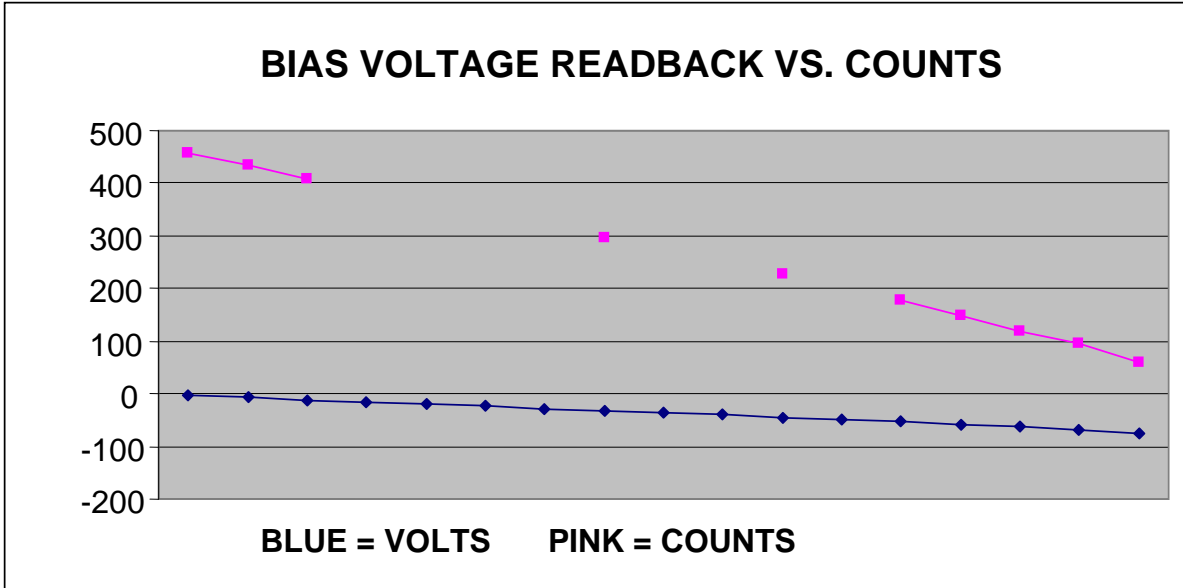
BIT12 = Switch 5-5

BIT13 = Switch 5-6

BIT14 = Switch 5-7

BIT15 = Switch 5-8





This chart illustrates the relationship between actual bias voltage and the read-back value for the main bias generator.

DRIVER STATUS TABLE – The 14 words are defined as follows;

Dn\_STAT ; STATUS VALUE FOR DRIVER n  
Dn\_TS1 ; DRIVER n, TEMP SENSOR #1  
Dn\_TS2 ; DRIVER n, TEMP SENSOR #2  
Dn\_TS3 ; DRIVER n, TEMP SENSOR #3  
Dn\_TS4 ; DRIVER n, TEMP SENSOR #4  
Dn\_TS5 ; DRIVER n, TEMP SENSOR #5  
Dn\_TS6 ; DRIVER n, TEMP SENSOR #6  
Dn\_TS7 ; DRIVER n, TEMP SENSOR #7  
Dn\_TS8 ; DRIVER n, TEMP SENSOR #8  
Dn\_VPP ; DRIVER n, VPP MONITOR  
Dn\_VNN ; DRIVER n, VNN MONITOR  
Dn\_BIAS ; DRIVER n, BIAS MONITOR  
Dn\_V25 ; DRIVER n, 2.5 VOLT MONITOR  
Dn\_V33 ; DRIVER n, 3.3 VOLT MONITOR

DRIVER STATUS WORD (Dn\_STAT) --The bits are defined as follows;

Board ID	BIT 0	LSB OF BOARD ID BIT
Board ID	BIT 1	BOARD ID BIT
Board ID	BIT 2	BOARD ID BIT
Board ID	BIT 3	MSB OF BOARD ID BIT
Empty Bit	BIT 4	ALWAYS 0
Empty Bit	BIT 5	ALWAYS 0
Empty Bit	BIT 6	ALWAYS 0
Empty Bit	BIT 7	ALWAYS 0
STAT_READY	BIT 8	DRIVER READY FOR COMMANDS
STAT_ACTIVE	BIT 9	ACTIVE MODE MIRROR ON BIAS
STAT_I2CFAIL	BIT 10	1 IF THE I2C BM IS BAD/TCD DIDNT ACK
STAT_TCDHMUTE	BIT 11	1 IF I2C BUS FAILURE/TCD FAILURE
STAT_OVERLOAD	BIT 12	1 IF AMPS APPROACHING RAIL
STAT_OVERTEMP	BIT 13	1 IF TEMPS ARE GETTING TOO HIGH
STAT_DRIVERFAIL	BIT 14	1 IF THE DRIVER HAS FAILED
STAT_INPUTBUS	BIT 15	1 IF INPUT BUS STATUS ACTIVE

BOARD ID: The Board ID bits give the board number that the status word is for, starting from '0000.' The first board will be '0000,' the second will be '0001,' up to the last board.

TEMPERATURE SENSORS: All Temperature read backs from the individual driver boards must be divided by 7. So in order to read the temperatures, it is recommended to convert the hexadecimal to base 10, then divide by seven.

VPP MONITOR: Convert to base 10 and divide by 20.

VNN MONITOR: Convert to base 10 and divide by -8.

BIAS MONITOR: See chart above "BIAS VOLTAGE READBACK VS. COUNTS."  
The driver reports the counts in hexadecimal. Convert to base 10 and use the chart to determine the voltage. This word only reports on BOARD 1, all other boards will report a '1.' This is only accurate when the bias is up, it will not report a correct number in STANDBY mode.

2.5 VOLT MONITOR: Convert to base 10 and divide by 200.

3.3 VOLT MONITOR: Convert to base 10 and divide by 200.

**'F', 0x46, 01000110B****ECHO BACK THE FRAME BUFFER**

RETURNS: 961 bytes total (maximum configuration 10 boards)

Packet length = 961 bytes

'F', 0x46, 01000110B	1 BYTE
DRIVER1 VOLTAGE TABLE	96 BYTES
DRIVER2 VOLTAGE TABLE	96 BYTES
.	
.	
.	
DRIVER 10 VOLTAGE TABLE	96 BYTES

Byte 0 is the packet identifier followed by the frame buffer contents low byte, high byte beginning with channel 0. This command is used to verify control bus communications by reading back what is contained in the driver frame buffer. It will only echo back the control bus frame buffer and not the input bus frame.

**'G', 0x47, 01000111B****ECHO BACK THE GAIN COEFFICIENTS**

RETURNS: 961 bytes total (maximum configuration 10 boards)

Packet length = 961 bytes

'G', 0x47, 01000111B	1 BYTE
DRIVER1 GAIN TABLE	96 BYTES
DRIVER2 GAIN TABLE	96 BYTES
.	
.	
.	
DRIVER 10 GAIN TABLE	96 BYTES

Byte 0 is the packet identifier followed by the gain buffer contents low byte, high byte beginning with channel 0. This command is used to verify control bus communications by reading back what is contained in the driver gain buffer. It will only echo back the control bus gain buffer and not the input bus frame. Since the gain value occupies the low byte of each channel read back. The high byte will be zero.

**'D', 0x44, 01000100B****READ THE DRIVER TYPE**

RETURNS: (3 bytes total)

'D', 0x44, 01000100B	1 BYTE
0x27	1 BYTE
0x00	1 BYTE

**'H', 0x47, 01000100B**                      **TOGGLE DISPLAY ROLL MODE**

RETURNS: '>', 0x2E, 00101110B                      ACK (1 byte)  
OR                      '?', 0x3F, 00111111B                      NACK (1 byte)

This command is used to turn off the event driven mode for the LCD and enable the rolling display mode.

**'J', 0x49, 01001001B**                      **SET DISPLAY CONTRAST**

RETURNS: '>', 0x2E, 00101110B                      ACK (1 byte)  
OR                      '?', 0x3F, 00111111B                      NACK (1 byte)

Range of 0 to 0xFFF; 0 = max contrast

**'Z', 0x44, 01000100B**                      **TOGGLE LIGHTS**

RETURNS: '>', 0x2E, 00101110B                      ACK (1 byte)  
OR                      '?', 0x3F, 00111111B                      NACK (1 byte)

Used to blank all light emissions from driver, including driver card status LED's and LCD backlight.

**'B', 0x42, 01000010B****SET MAIN BIAS VOLTAGE**

Must send 2 byte argument (3 BYTES TOTAL)

LB, HB See table below for voltage vs. 'B' command = 10.5 to 70 volts

RETURNS: (1 byte total)

RETURNS: '>', 0x2E, 00101110B ACK (1 byte)

OR '?', 0x3F, 00111111B NACK (1 byte)

\*\* Must be done from MANUFACTURING MODE. Must be performed after bringing the bias up in ACTIVE mode by issuing a '1' command. This command will bring the bias up from STANDBY mode, however when you go ACTIVE you will revert back to the default bias (-50 V). So in order to set the bias, go ACTIVE in MANUFACTURING mode, and issue the 'B' command as described here.\*\*

Xinetics has tested the following 'B' command bias settings

<b>'B' Command</b>	<b>Bias Setting</b>
0x300	10.5 V
0x2FF	25.1 V
0x1FF	34.6 V
0x159	50.2 V
0x0FF	58.6 V
0x0F0	60.0 V
0x0B4	65.7 V
0x08C	69.4 V
0x082	70.3 V

**'Y', 0x59, 01011001B****SET INPUT BUS MODE**

Must send 1 byte argument (2 BYTES TOTAL)

This parameter cannot be modified when driver is in the ACTIVE mode.

Y2 = INPUT BUS OFF

Y3 = INPUT BUS ON SOR-422 MODE

Y4 = INPUT BUS ON XIBUS MODE

RETURNS: (1 byte total)

'>', 0x2E, 00101110B 1 BYTE (ACK)

'?', 0x3F, 00111111B 1 BYTE (NACK)

**'M', 0x4D, 01001101B**

**SET DRIVER MODE**

Must send 1 byte argument (2 BYTES TOTAL)

This parameter cannot be modified when driver is in the ACTIVE mode.

MT = TEST MODE (half gains)

MN = NORMAL MODE (full gains)

RETURNS: (1 byte total)

'>', 0x2E, 00101110B 1 BYTE (ACK)

'?', 0x3F, 00111111B 1 BYTE (NACK)

**'I', 0x49, 01001001B****INPUT A FRAME**

Must send 2 byte argument plus the frame (962 BYTES TOTAL)

Note, packet length can be modified with the C command if desired

ID = INPUT A DATA FRAME (VOLTAGES)  
 IG = INPUT A GAIN FRAME  
 IO = INPUT AN OFFSET FRAME

ID Data values are 16 bit low byte / high byte beginning with channel 0

IG Data values are 16 bit low byte / high byte, 8 MSB's are ignored

IO Data values are 16 bit low byte / high byte, 6 MSB's are ignored

RETURNS: (1 byte total)

'>', 0x2E, 00101110B 1 BYTE (ACK)

'?', 0x3F, 00111111B 1 BYTE (NACK)

**Data Frame Format:**

Data Frame Format is what is known in the industry as two's complement. The MSB is the sign bit and the 15 LSB's determine the magnitude of the voltage. If the MSB is a 1, the output voltage will be negative.

Data input format is defined as follows:

VALUE	OUTPUT VOLTAGE (test)	OUTPUT VOLTAGE (normal)
0x7FFF	+15 volts ± offset	+30 volts ± offset
0x4000	+7.5 volts ± offset	+15 volts ± offset
0x0000	0 volts ± offset	0 volts ± offset
0xC000	-7.5 volts ± offset	-15 volts ± offset
0x8000	-15 volts ± offset	-30 volts ± offset

**Gain Frame Format:**

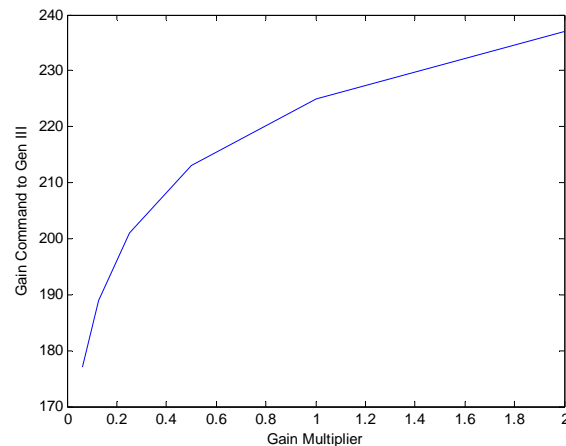
The driver must be in NORMAL mode or this command will not take effect. It will be ACKed in TEST mode, but will not actually upload the Gain Frame. The gain values are 8-bit values. In order to maintain the driver protocol, 16 bit values must be transmitted, however only the 8 LSB's will be used by the driver for a gain frame. The 8-bit value in each word represents the gain for the corresponding channel. Xinetics has tested the gains provided in the table below. From that table, other values can be interpolated or calculated. Note that the relationship between the commanded gain and the gain multiplier is not linear, please see the graph below.

When the driver is turned on, the default value for the gains will read as '0xD5.' This gain value is \*not\* valid as it is described in this section. This default value will produce the responses in NORMAL and TEST modes as described above in the 'ID' Data Frame Format section. After a gain frame has been sent to the driver, or the 'IG' command has been invoked in any way, the

defaults are erased and the values described in this section take effect. So to return to the default settings, in NORMAL mode a 0xE1 must be sent, not the default 0xD5. Or, powering down and restarting the Gen III will restore the defaults.

The following table provides some common voltage and gain values for a data input (ID) of 0x4000 (half scale positive, or +15 V) in NORMAL MODE:

Gain Value	Gain Multiplier	Output Voltage
0xED	2	+30 volts $\pm$ offset
0xE1	1	+15 volts $\pm$ offset
0xD5	.5	+7.5 volts $\pm$ offset
0xC9	.25	+3.75 volts $\pm$ offset
0xBD	.125	+1.87 volts $\pm$ offset
0xB1	.0625	+.937 volts $\pm$ offset



Note: It is possible to program a gain that will cause the amplifier to rail; this can result in unpredictable behavior due to math overflows in the DSP. The total commanded voltage is a value dependent on input value, gain and offset. The DSP uses these values along with the power supply rail values to compute a pulse width that drives the actuator. The power supply rails are factory set to  $\pm 34$  volts and require at least two volts of overhead to function properly. Do not command a voltage greater than  $\pm 32$  volts without contacting Xinetics for procedures on how to adjust the power supply rails in the driver system. Power supply rail voltage directly impacts quiescent power in the driver. The fans will servo to a higher value to compensate for the increased power dissipation if the power supply rails are increased.

### Offset Frame Format:

Offset values are represented by a 10 bit number (low byte / high byte right justified). This means that although the user will transmit offset values of 16 bits, only the least significant 10 bits of the value will be used.

The format for the offset is twos complement and the MSB (bit 9) is the sign bit. The default offset loaded by the system is 0x00 and usually results in an output within 100 mV of 0 when the



input is commanded to mid scale. If higher accuracy or operation within 100 mV of the rail is required, then the offset can be adjusted to zero the mid scale value. The offset resolution is 5 millivolts per LSB and the total offset range is  $\pm 2.5$  volts.

Some typical offset values are given in the following table.

Offset Value	Offset Voltage
0x200	-2.5 volts
0x3FE	-.010 volts
0x3FF	-.005 volts (-1 LSB)
0x000	0 volts
0x001	+.005 volts (+1 LSB)
0x1FF	+2.5 volts

Note that the offset is not affected by the gain so a 1 pass algorithm should be sufficient to achieve calibration. It can be seen that by manipulation of the offset and gain registers the driver system may be calibrated for virtually any operational requirements.

### **\*\*\*MANUFACTURING mode should be used with caution\*\*\***

Important safety features are disabled when in MANUFACTURING mode that could result in damage to the driver system or a mirror.

To enter Manufacturing mode, the driver must be in STANDBY mode, issue the 'MM' command over the command bus. The driver will respond with an ACK. The LCD will show MANUFACTURING MODE in the status area. The LCD will show 8 information screens instead of the usual 4; these additional screens are cooling status, bias status, power supply status, and software Rev. information.

Additionally, when the system is in MANUFACTURING mode, all command interlocks are disabled. Also several test commands are enabled, namely 'O' for an odd waffle, 'E' for an even waffle and 'R' for a ramp and 'N' for hard mute are available. Bus modes and operating parameters can be set without putting the driver in STANDBY mode. There should never be a mirror connected to the driver when using MANUFACTURING mode. Note that all of the mirror protection features are disabled in manufacturing mode. Manufacturing mode is intended for driver system testing only.

The bias target and gain settings are held from the last mode enabled. In other words, if MANUFACTURING mode was entered from TEST mode, the bias target will be the TEST MODE BIAS and the gain will be set to  $\pm$  half scale. If MANUFACTURING mode was entered from NORMAL mode, the bias target will be set to the NORMAL MODE BIAS and the gains will be set to full.

**Manufacturing mode enhanced command set (controller):**

**‘M’, 0x4D, 01001101B                      SET DRIVER MODE**

Must send 1 byte argument (2 BYTES TOTAL)

MT = TEST MODE  
MN = NORMAL MODE  
MM = MANUFACTURING MODE

RETURNS:                      (1 byte total)  
‘>’, 0x2E, 00101110B                      1 BYTE (ACK)  
‘?’, 0x3F, 00111111B                      1 BYTE (NACK)

The following commands place frames into the buffer. The gain mode applies, in other words; if MM was entered from TEST mode, then half gains are loaded and the waffle will be  $\pm 7.5$  volts (give or take the offset) and if MM was entered from NORMAL mode, then full scale gains will be applied and the waffle pattern will be approximately  $\pm 15$  volts.

**‘E’, 0x45, 01000101B                      LOADS THE EVEN WAFFLE PATTERN**

RETURNS:    ‘>’, 0x2E, 00101110B                      ACK (1 byte)  
OR            ‘?’, 0x3F, 00111111B                      NACK (1 byte)

Places a 0x4000 count even waffle pattern in the frame buffer

**‘O’, 0x4F, 01001111B                      LOADS THE ODD WAFFLE TEST PATTERN**

RETURNS:    ‘>’, 0x2E, 00101110B                      ACK (1 byte)  
OR            ‘?’, 0x3F, 00111111B                      NACK (1 byte)

Places a 0x4000 count odd waffle pattern in the frame buffer

**‘R’, 0x52, 01010010B                      LOADS THE RAMP PATTERN**

RETURNS:    ‘>’, 0x2E, 00101110B                      ACK (1 byte)  
OR            ‘?’, 0x3F, 00111111B                      NACK (1 byte)

Places a ramp starting at  $-$ half scale to  $+$  half scale into the frame buffer

**‘N’, 0x4E, 01001110B                      HARD MUTE ALL OF THE DRIVER CARDS**

RETURNS:    ‘>’, 0x2E, 00101110B                      ACK (1 byte)  
OR            ‘?’, 0x3F, 00111111B                      NACK (1 byte)

Ramps down the gains and hard mutes the amplifiers

**‘[’, 0x5B, 01011011B            DECREASE BIAS TARGET BY 1 VOLT**

RETURNS:    ‘>’, 0x2E, 00101110B            ACK (1 byte)  
OR            ‘?’ , 0x3F, 00111111B            NACK (1 byte)

**‘]’, 0x5D, 01011101B            INCREASE BIAS TARGET BY 1 VOLT**

RETURNS:    ‘>’, 0x2E, 00101110B            ACK (1 byte)  
OR            ‘?’ , 0x3F, 00111111B            NACK (1 byte)

## Glossary of terms:

Switching Amplifier	- Refers to a class D amplifier which is controlled digitally.
Power Processor	- The controller part of the Xinetics chip set that uses $\Delta$ - $\Sigma$ modulation to generate a PSM spectrum for FET drive.
PSM	- Power Spectrum Modulation, a proprietary form of switching waveform used to increase efficiency.
Slew Rate	- The ultimate voltage response of the amplifier, slew rate is dependent on output current and capacitive loading.
Settling time	- The time it takes from when the amplifier starts to slew until the voltage at the actuator has settled to 16 bits.
Latency	- The time it takes for the signal processing chain to process a command and direct the amplifier to begin a slew.
Frame Rate	- The speed at which input commands are processed.
Bandwidth	- The total time for the command to be processed and the load to settle on the new voltage (frame time + latency + settling time)
Control Bus	- The bidirectional serial bus used to control the driver system.
Input Bus	- The high speed parallel input bus used to input mirror data.
Xibus	- A proprietary input / output SERDES bus used for interface to the driver chassis.
SERDES	- Serializer / Deserializer
PSD	- Power Spectrum Distribution
SOR-422U	- The LVDS input bus specification.
NORMAL Mode	- The driver mode that allows full amplitude signals to be applied to the mirror.
TEST Mode	- The driver mode that allows a safe level of drive to be applied to the mirror for verification of system functionality.
MANUFACTURING Mode	- A driver mode for Xinetics use only, used for testing and setup of the driver electronic systems.
ACTIVE Mode	- The system is actively driving the mirror.
STANDBY Mode	- The system is idle and not driving the mirror
CONFIG Mode	- The system is performing mapping and test functions internally
BIAS	- The voltage applied to the low side of the actuator array to bias the PMN into the active region.
ACK	- The byte returned from the driver to signal that the command was processed successfully.
NACK	- The byte returned from the controller to signal that there was a command error.
Frame	- A formatted packet of data pertaining to the control of a group of channels.
Gain	- The amplification factor applied to each channel.
Offset	- The voltage offset value applied to each channel.
Calibration	- The process of sending gain and offset frames to the driver to maximize dynamic range and accuracy.